Docket No.: 3672-0144P
(PATENT)

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael O. THOMPSON et al.	**Before the Board of Appeals**
Application No.: 10/088,913	Confirmation No.: 8909
Filed: May 7, 2002	Art Unit: 2824
For: NON-VOLATILE PASSIVE MATRIX DEVICE AND METHOD FOR READOUT OF THE SAME	Examiner: J. H. HUR

APPEAL BRIEF

MS Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As required under § 41.37(a), this brief is being filed after the filing of the Notice of Appeal, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2), and any required petition for extension of time, if applicable, for filing this brief and fees related thereto, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

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APPEAL BRIEF ON BEHALF OF APPELLANT: Michael O. THOMPSON et al.

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Sir:

I. REAL PARTY IN INTEREST

The real party in interest for this application is the Assignee, Thin Film Electronics ASA, P.O. Box 1872 Vika, N-0124 Oslo, Norway.

II. RELATED APPEALS AND/OR INTERFERENCES

There are no related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-18 are currently pending in this application wherein claims 6-11 have been withdrawn from consideration. Claims 1, 12 and 13 are independent. The final Office Action dated January 08, 2008 rejects claims 1, 13, 14, 16 and 17 under 35 U.S.C. 103(a) in view of

Kuroda (U.S. Pat. No. 5,487,029) and Clemons (U.S. Pat. No. 4,599,709); claims 12, 15 and 18 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Seyyedy (U.S. Pat. No. 5,969,380) and claims 2-5 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Dierke (U.S. Pat. No. 5,734,615).

Claims 1-5 and 12-18 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No further amendments have been presented after the outstanding Office Action of January 08, 2008.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

With respect to independent claim 1, the claimed invention is directed to a non-volatile passive matrix memory device in which the memory matrix which will allow for massive parallel readout at a high data rate with a reduction in the number of sense amplifiers necessary for such a massive parallel readout. There is no limit to the number of bit lines and therefore the memory matrix can be as large as necessary. The memory matrix is defined by a set of crossing word lines and a set of bit lines (see figs. 5 and 6). A memory cell is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix. A passive memory requires each memory cell be at all times in physical ohmic contact with a word line and a bit line. See specification pages 7-9 and Figs.1 and 2.

The word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position

within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means. This enables simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment. See specification pages 10 -11[1].

With respect to claim 12, the claimed invention is directed to a volumetric data storage apparatus, in which a plurality of stacked layers includes a non-volatile passive matrix memory device. The memory matrix allows for massive parallel readout at a high data rate with a reduction in the number of sense amplifiers necessary for such a massive parallel readout. There is no limit to the number of bit lines and therefore the memory matrix can be as large as necessary. The memory matrix is defined by a set of crossing word lines and a set of bit lines (see figs. 5 and 6). A memory cell is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix. A passive memory requires each memory cell be at all times in physical contact with a word line and a bit line. See specification pages 7-9 and Figs.1 and 2.

The word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means. This enables simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment. See specification pages 10 -11[2].

With respect to independent claim 13, the claimed invention is directed to a memory device, whereby the memory matrix allows for massive parallel readout at a high data rate with a reduction

[1] *Specific reference to page 10 lines 15-21*

in the number of sense amplifiers necessary for such a massive parallel readout. There is no limit to the number of bit lines and therefore the memory matrix can be as large as necessary. The memory matrix is defined by a set of crossing word lines and a set of bit lines (see figs. 5 and 6). A memory cell is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix. A passive memory requires each memory cell be at all times in physical contact with a word line and a bit line. See specification pages 7-9 and Figs.1 and 2.

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VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Final Office Action provides the following ground of rejection for review on appeal:

(a) Claims 1, 13, 14, 16 and 17 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029) and Clemons (U.S. Pat. No. 4,599,709); and

(b) Claims 12, 15 and 18 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Seyyedy (U.S. Pat. No. 5,969,380).

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[2] *Specific reference to page 10 lines 15-21*
[3] *Specific reference to page 10 lines 15-21*

VII. ARGUMENTS

A. The Rejections Fail to Establish *Prima Facie* Obviousness of Independent Claims 1, 12 and 13

1. Argument Summary

The Examiner's reasoning provided in support of the rejection of independent claims 1, 12, and 13 under 35 U.S.C. §103(a) as being obvious under the combination of *Kuroda* in view of *Clemons* and with respect to claim 12 *Seyyedy,* fails to establish *prima facie* obviousness. Specifically, the examiner has failed to provide references that teach or suggest all of the claim features. The Examiner has failed to provide references that refer to teaching of passive matrix memories and their characteristics. Instead, the Examiner provides references that teach active and other memories.

2. The Relied Upon References, Kuroda, Clemons and Seyyedy, Do Not Teach All the Claimed Elements Recited in the Independent Claims.

a. Difference Between Passive, Active and Other Memories

Appellants respectfully submit that the teachings of the applied references Kuroda, Clemons, and Seyyedy teach active memory devices or other types of memory devices all of which are entirely different from a passive matrix memory array of the claimed invention. These differences lead to a disconnect between the teachings of the references and the claimed elements. In illustrating this point, Appellants discuss the differences between the various types of memories in order to help point out the Examiner's error in applying each reference.

The present invention concerns a passive matrix-addressable ferroelectric or electret memory. This of course follows from the fact that the memory is an electrically polarizable dielectric material exhibiting hysteresis. Moreover the memory device according to the invention is a passive device, i.e. all the memory cells of the memory array is contacting the electrodes

permanently. This contrasts with an active matrix-addressable memory, wherein each memory cell comprises a switching means, usually a FET transistor for establishing an electrical circuit between the memory cells and for instance its bit line electrode. This means that while all the memory cells of a passive matrix-addressable memory permanently are connected in an RC network, in an active matrix-addressable memory a memory cell selected for an addressing operation, i.e. a write or read operation, is switched into the network by switching means connected with a memory cell.

Both types of memory have their advantages and disadvantages. In a passive matrix-addressable memory a write or read operation consists in applying a switching voltage or potential over a selected memory cell and record a charge or current output response on the bit line by means a sense amplifier connected thereto. The so-called switching voltage which is applied for an addressing operation is usually selected much larger than their coercive voltage of the memory material. This implies that as an average a memory cell will be switched in 50% of the addressing operations, i.e. its polarization direction will be reversed. This amounts to a destruction of the datum stored in the memory cell, such that for instance a stored logical 0 will be switched to a logical 1. In such cases a memory cell has to be reset by performing a writing operation and this is done by once more applying a switching voltage to the memory cell, but of the opposite sign. In a passive matrix-addressable memory an addressing scheme with destructive write and read sets up so-called sneak currents and disturb voltages in the permanent RC network formed by the memory cells of the array. This in addition to parasitic or stray capacitances that are bound to occur, and in sum these effects may either change the set polarization state of a memory cell and cause spurious output responses on the bit lines in a read operation.

As well known to persons skilled in the art the unfortunate effects of destructive write and read in a passive matrix addressable array is abated by for instance subjecting all addressing operations to a so-called voltage pulse protocol and the use of an appropriate voltage selection rule which will serve to minimize potential differences on unselected memory cells during an addressing operation.

The unfortunate effects in connection with the destructive write and read operation are avoided in active matrix-addressable memories, since only a selected memory cell is connected to a word line and a bit line. Usually such memory cells are termed 1T-1C memory cell, which denotes a memory cell with one switching transistor and one ferroelectric capacitor (for instance). Other configurations are known, e.g. memory cells of the type 2T-2C etc. The penalty of this is that the use of switching transistors in an active matrix tends to be power-consuming and moreover makes the memory array larger and more complicated. Also the number of electrode lines is doubled, as selection lines for the gate electrodes of the switching transistors will be needed and the data has to be output on a data line, which is joined to one memory cell electrode, i.e. one of the plates of the capacitor formed by the memory cell, upon switching the transistor channel to conduction. The data line is then for instance connected to the drain contact of the switching transistor. The bit line proper is then the electrode that connects one or more e.g. ferroelectric capacitors with the source contact of the switching transistor. It should furthermore be noted that even an active matrix-addressable array is not completely free from parasitic capacitances, which by the way is a well-known problem in integrated circuit technology.

Generally ferroelectric memories have a much slower response than semiconductor memories such as DRAMs and SRAMs and hence the ferroelectric memories are better suited for use as ROM and WORM (Write Once, Read Many times). It should also be noted that in ferroelectric memories the data content cannot be erased, i.e. the memory cannot be set to a virgin state, but is non-volatile in the sense that a polarization state in principle could be maintained indefinitely and only completely erased by raising the temperature of the memory above the Curie temperature of the ferroelectric material, something which will return the material to its paraelectric phase. However, the fairly slow response of a ferroelectric memory can be offset by reading a large number of memory cells in parallel. In principle all memory cells on a word line can be read simultaneously, provided that each bit line is connected with a sense amplifier. Now there is also a penalty for this.

While ferroelectric memory arrays can be made extremely large, comprising millions or even hundred of millions of memory cells, it has turned out that it is difficult to operate a memory with more that 2000 word lines. In this case each bit line will be permanently connected in the passive configuration to no more than 2000 memory cells. One reason for this is the occurrence of floating charges on the bit line, a problem that aggravates with the number of memory cells on the bit line, and while it could be tempting to lower the access rate so that floating charges may decay, this would make the memory intolerably slow to operate. So the number of word lines is for practical reasons the typical ferroelectric memory material limited to about 2000, the exact number being dependent on the actual ferroelectric memory material used.

The capacity of memory can, however, be increased by resorting to a large number of bit lines, e.g. 16000 or 32000, which would respectively produce a memory array of 32 or 64 million memory cells. Performing a parallel readout of all memory cells on a word line in the latter case would imply that each bit line is connected with a sense amplifier, making 32000 sense amplifiers all told. It is easily seen that this would even with a slow response time of 1 μs yield a data rate corresponding to 32 GHz. There are several reasons why this arrangement is not desirable. One is the problem of handling this data rate, the other is the very large number of sense amplifiers that is needed, and considering that a sense amplifier usually comprises two operation amplifiers, this implies at least 50 to 60 transistors for each sense amplifier. However, a more than adequate data rate would be 1 GHz, which would be competitive with fast DRAMs and SRAMs and would then, of course, imply parallel read of 1000 bit lines at once. Typically a data word read in this manner shall consist of 1 K bits or 128 bytes. By dividing the word line into segments of say 1024 memory cells a correspondingly large data word may be read in about 1 μs by connecting all the bit lines forming the word line segment to sense amplifiers. As a consequence a number of sense amplifiers can be reduced to the number of bit lines in a word line segment and with obvious advantages. This is precisely what the present invention discloses. Such an arrangement is not known in the prior art, and is neither anticipated nor suggested in any or the prior art documents cited by the Examiner.

Appellants have provided attachments[4] A/1 through D/11 which describe various types of memory architecture and provide the following discussion of each. Attachment A/1 discloses a conventional active ferroelectric memory as known in the art. Specifically it depicts a memory with four memory cells, each of which comprises a ferroelectric capacitor and a switching transistor. Hence the memory cells are of the type IT-IC. Memory cell types with more transistors and more capacitors are, however, known for instance a 2T-2C memory cell. Bit lines 314 are each connected with a sense amplifier, while two sets of word lines are used, namely those marked SWL which are used for gating the switching transistors of each memory cell 302 as well as driving word lines or pulsing word lines PWL connected both with a memory control logic as well as a source contact of additional switching transistor 315, one of which is provided for each pulsing word line. On accessing a memory cell the select word line SWL is pulsed high at the same time as the pulsing word line PWL connected with a memory control logic is also pulsed high. The word line switches 315 are of course jointly gated from the switching word line SWL and as a result the pulsing word line PWL goes high. The capacitor of the selected memory cell discharges through the now conducting switching transistor of the memory cell and to the bit line or data line 314, outputting a charge or current response from the selected memory cell to be sensed by the sense amplifier 206. The arrangement depicted in the enclosed figure 3a allows for a parallel readout on both memory cell collected to one and the same pulsing word line PWL, i.e. all memory cells in a row. As will also be seen, only the selected memory cells have their capacitors temporarily in ohmic contact with the electrodes. Hence no voltage disturb to the unselected memory cells are generated. Persons skilled in the art will furthermore realize and know that also the active matrix-addressable array in fig. 3a can be provided without parallel access, i.e. only a single memory cell can be selected at a time and brought into ohmic contact with the electrode. This shall however, necessitate an additional bit line or data line, one of which connects to the sense amplifier for readout.

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[4] *Attachments A/1 – D/11 are found in Appendix D*

Fig. 3b on sheet B/1 depicts a passive ferroelectric memory. Memory material of the memory cell indicated by 315 in fig. 3b is provided between word line electrodes 310 and bit line electrodes 314 where they cross to form a matrix of passive addressable memory cells formed in memory material between the crossing of electrodes 314 and 320. Note that the ferroelectric memory material, which is a dielectric, can be provided as a global layer between the electrodes 310 and 314. A ferroelectric capacitor is shown schematically in fig. 4, and 315 depicts the ferroelectric thin film interspersed between metal electrodes, e.g. word lines 310 and bit lines 314. As will be seen, the dielectric material, i.e. the ferroelectric material of the capacitor, is at all times in ohmic contact with the metal electrodes. The problem with this is that when a memory cell for instance as depicted at the crossing 320 is selected for write and read, a switching of the polarization of this memory cell shall cause a voltage disturb to all the remaining cell in the array, something which may result in floating capacitances on the bit line, spurious readout values and in the worst cases inadvertent switching of unselected memory cells, thus changing their polarization states and altering the logical values of the data stored. The ferroelectric material may be inorganic, typically a perovskite, or organic, typically a polymer or copolymer of vinylidene fluoride. Such a polymer spontaneously forms a diode junction to one of the electrodes as depicted at 322, thus blocking a charge flow in an opposite direction. In case of an inorganic ferroelectric material a thin layer of a semiconductor, e.g. gallium arsenide, may be provided between the ferroelectric thin film and a metal electrode in order to create a Schottky diode junction.

A static random access memory is documented on attachments C/1-C/5 as downloaded from Wikipedia and herewith enclosed. This is the type of memory cell used in Clemons which explicitly is stated to be an SRAM. SRAMs are usually organized in CMOS architectures as depicted in the figure in C/2 and comprise six transistors, viz. 2 access transistors and 4 memory transistors in the form of two cross-coupled inverters M1-M4. They form the bistable latching circuit used to store a bit and the stored bit is retained by an SRAM as long as the memory circuit is powered. Hence no periodical refresh is required as is the case of a dynamic random access memory. Disturb of the memory cells is of course no issue here, but note that the configuration

shown uses two bit lines, although it is possible to come away with only one. Two bit lines are, however, used as it will allow for differential signaling and highly improve the signal-to-noise ratio. Compared with both active ferroelectric memories and passive ferroelectric memories a SRAM has a much lower integration and consumes far more real estate, typically 6 times as much as a high density passive ferroelectric memory cell, in addition to also being more power consuming.

Attachments D/1 -D/11 show a true hybrid between a ferroelectric memory cell and conventional CMOS-based random access memories, namely a FERAM. As known by persons skilled in the art, a DRAM includes both signal transistors as well as capacitors and need to be continually refreshed. A SRAM memory cell has at least four storage transistors as well as two access transistors, while active matrix-addressable ferroelectric memories may have a memory cell with one access transistor or one storage capacitor.

Finally, we have the passive ferroelectric memory cell as used in the present invention. Both DRAM and FERAM use a capacitor and switching transistors of the memory cell proper. In both cases it is similar to that of the l T-1 C type and hence comparable to an active ferroelectric memory. Both FERAM and an active ferroelectric memory differ from a DRAM as they similarly to the SRAM have no need for refresh (and the ferroelectric memory is of course truly non-volatile). The same of course also is valid for a passive ferroelectric memory. The big advantage of a FERAM seems to lie in the fact that it can be configured to be read non-destructively as apparent from D/1 to D/5. This is due to the fact that the direction of the remanent field of the ferroelectric capacitor which is provided as the gate insulator between a gate electrode and a transistor channel actually influence the source/drain current by affecting the movement of charges in the semiconductor substrate, i.e. speed and direction. This results in a different current output response from the transistor without the need for applying a switching potential across the ferroelectric material and between the gate electrode and the transistor channel. Writing, i. e. changing the polarization state of the FERAM must take place as with conventional ferroelectric memories, namely by applying a

switching potential or not depending on whether the polarization state shall be changed or not in the writing process.

b. Teachings of Kuroda

The Examiner has provided Kuroda to teach the use of a passive matrix memory. The Examiner implies that blocks (1,1)...(1,7) shown in Fig. 1 provide a passive matrix memory array because each intersection of word and bit lines includes only a capacitor but no switching means. However, a passive matrix memory requires the ferroelectric material of the capacitor be at all the time are in ohmic contact with the metal electrodes. **Appellants recite this language explicitly within claims 1, 12 and 13 which is not taught by Kuroda.**

Kuroda does not teach this and in fact teaches to the contrary. First, nowhere does Kuroda teach or suggest that it provides a passive matrix memory. Further, nowhere does it teach characteristics that conform to a passive matrix memory. To the contrary a person skilled in the art would contemplate Kuroda and observe that the stated object in Kuroda is to improve on an active matrix-addressable memory by increasing its integration and by reducing the overall voltage disturb, which Kuroda terms the voltage stress. The increased integration is achieved by instead of having for instance an IT-IC memory cell, resorting to a memory circuit with one switching transistor capable of switching memory cell, for instance shown as Q1, Q2, Q3 and so on. These memory circuits actually comprises 8 memory cells as depicted by their capacitors shown with one electrode connected via the source contact of the switching transistor Q1. In other words, Kuroda provides a true active memory circuit, and each capacitor of a circuit of course corresponds to a bit spot or a memory cell.

Further, it is a stated objective of Kuroda to appreciably reduce the voltage disturb as compared with a passive matrix-addressable memory cell. This is achieved by selecting a single memory circuit of a block, for instance block (1,0) in fig. 1, at a time and then selecting a single memory cell of this memory circuit for write and read to be preformed via a write/read control

logic circuit WRCO with one sense amplifier SA and one write amplifier WA. The selection of a memory circuit takes place by pulsing the selection word line WB1 high and similarly setting either a data line DO, D1... high or a word line W10...W17 high with a resulting charge or current response from the memory cell connected to one of the word lines W10-W17 of each of the 8 memory cells of a memory circuit.

An X decoder XDEC and a Y decoder YDEC are provided in addition. All blocks of a column are connected via a multiplexer arrangement (YSELECT) with appropriate switching transistors Q4...Q9 and so on to the write/read control circuit WRC. This write/read control circuit WRC is moreover used to apply a voltage pulse protocol with a half voltage selection rule in order to further enhance the disturb strength of this memory. Table 1, col. 16-17 of Kuroda illustrates where Kuroda distinguishes between the memory of his invention and known prior art memories. In this table Prior Art 1 conforms to a wholly passive ferroelectric memory, i.e. with no switching elements at all and similar to the present invention, Prior Art 2 conforms to a fully active ferroelectric memory with cells of the I T-I C type and finally Prior Art 3 evidently to for instance a ferroelectric memory of the active type with memory cells for instance of the 1T-2C type and so on. The latest prior art could be seen as an advance towards the approach taken by Kuroda, but differs essentially from Kuroda as Kuroda discloses the memory circuit with 8 capacitors and one switching transistor, thus with one capacitor for each memory cell. The main difference here is of course the blockwise arrangement of Kuroda which can be regarded as essential to achieving the desired low voltage disturb. As given at the bottom of column 17 and the top of column 18 of Kuroda, it is seen that his invention provides a disturb coefficient which can be given as 1.006. This is of course not much higher than the unity disturb coefficient of an active matrix-addressable array, while the disturb coefficient is in a passive matrix-addressable memory as used with the present invention is given as 1.025 and apparently correspondingly high in the configuration according to Prior Art 3. Relevant here is that with regard to disturb, Kuroda for all practical purposes is identical with the active matrix-addressable memory, but by reducing the number of switching transistors to 1/8 of the relevant prior art, he is able to achieve a correspondingly higher integration.

Thus, while the use of capacitors at the junction between a word and bit line in the bitewise arrangement of Fig. 1 appears in the doorway to represent a passive matrix memory architecture on the surface, the facts as disclosed by Kuroda suggest an active matrix memory. Thus, based on these facts one of ordinary skill would also presume that Kuroda teaches an active matrix memory and not use it for teaching a passive memory as claimed.

c. Teachings of Clemons

Clemons concerns a completely different kind of memory, namely a semiconductor memory of the SRAM type and a multi-bit organization. Clemons discloses how to achieve a memory architecture tailored to a bytewise organization by dividing the memory into block-like arrangement such that all bits of a byte accessed in a given operation are obtained from physically adjacent columns referred as byte blocks and thus distinguished above input/output blocks in prior art, see Clemons col. 4, lines 40-45. Clemons teaches nothing more than providing a bytewise-organized memory by defining blocks of the memory in terms of a bytewise arrangement made up of adjacent data lines such that, for instance, a byte may be read in parallel from one row of memory cells in a block at a time.

In consideration of the complexity of the various memory devices, Appellants have attached hereto a table[5] labeled as table 1 highlighting the differences between, Kuroda, Clemons, the alleged combination of Kuroda and Clemons as compared to the present invention.

3. One of Ordinary Skill Would Not Combine the Teachings of Clemons with Kuroda to Achieve Appellants Claimed Invention

a. Kuroda Does Not Teach or Suggest Parallel Read Out – One of Ordinary and of Common Sense in the Art Would Not Conclude it Obvious to Try to Force Parallel Readout on Kuroda's Memory by Combining it with Clemons Teachings

[5] *Table 1 is found in Appendix D*

Kuroda does not allow for parallel readout. Only a single memory cell of a single circuit in one block of a column of blocks is read at a time. As already stated, the Y-SELECT block is used to multiplex the data lines to connect with the sense amplifier SA (or write amplifier WA) in the write/read control circuit WRC at the bottom of each column. In principle of course a parallel read could be obtained in Kuroda by allowing in the simultaneous reading of one memory cell in each block and on one and the same word line (row) via the single sense amplifier provided for each column. This would amount to reading an eight-bit byte in parallel, but would then nullify the expressly stated object of Kuroda to keep the voltage disturb or voltage stress coefficient low. Attempting parallel readout in this manner would actually *increase* the disturb coefficient by a factor of 8.

Kuroda discloses essentially a very small memory capable of storing only 1024 bits, but with very high integration factor. These memories could be realized with extremely small dimensions and should hence be eminently suited for the applications as indicated in Figs. 56-59, where they are shown provided in great numbers and distributed in respective technological systems such as automobiles, airplanes, space stations and rockets to handle measurement and control functions. Hence the low storage capacity is offset by being able to provide one highly integrated memory chip for each function.

Moreover it is no doubt that the architecture and mode of operation envisaged by Kuroda, namely an access rate of one bit at a time from each memory, shall to a high degree serve to contribute their reliability in the applications as envisaged and illustrated in Kuroda. Such desirable properties would however, be nullified if one attempts to modify Kuroda with multiplexing arrangements for parallel readout, either of one bit simultaneously from each column or of one bit simultaneously from each memory circuit of a block in a column. This latter would be exactly what the Examiner proposes to do, namely taking a known multiplexing arrangement from Clemons and used in this prior art SRAM device dating from 1984 to achieve a bytewise organization in the ferroelectric memory disclosed by Kuroda. Indeed the Examiner has to go further as components such as the Y-

SELECT blocks and their WRC circuits now have to be removed from Kuroda and replaced by the multiplexer arrangement of Clemons. But the Examiner gives no hint whether spares are now to be included in Kuroda also. This would indeed have been a sensible move since the proposed hypothetical memory circuit with the multiplexing arrangement of Clemons would have an increased voltage disturb coefficient and lowered reliability.

Hence the prior art ferroelectric memory of Kuroda might be modified by the multiplexer arrangement of Clemons to yield a bytewise parallel read and write, but at the price of throwing out both the selector blocks and the write/read control circuits of Kuroda and ending up with a ferroelectric memory with about the same integration factor, but unfortunately with an eightfold increased voltage disturb coefficient. A person skilled in the art contemplating the teachings of Kuroda could not be led to the hypothetical memory circuit suggested by the Examiner as the resulting memory circuit would not fulfill its objectives. With a much higher voltage disturb coefficient it would not be suited for the applications envisaged by Kuroda which presupposes a very high reliability memory circuit. In this connection note that FEM (ferroelectric memories) are non-volatile as opposed to the SRAM, also in the sense that they retain the stored datum in case of a power loss. This would not be the case of an SRAM.

Since Clemons is not at all concerned with ferroelectric or electret memories, but rather a semiconductor SRAM memory, it is a dubious claim that Clemons teachings can be hoisted on Kuroda. The teaching of Clemons would actually ruin the expressed object of Kuroda as it would demand that all 8 memory circuits of a block in Kuroda's memory should be selected and connected, for example, a write or read operation. This would increase the voltage stress ratio of Kuroda's memory eightfold, but in addition it would also serve to make Kuroda's memory rather more complicated as it would need a complete rearrangement of the Y-Select block as well as the Write/Read Control Block(WRC). The latter must for instance be equipped with 8 sense amplifiers, but even this would not transform Kuroda's device into one similar of the present invention, with regard to operational features, as further multiplexing arrangements would be needed if for instance

the Write/Read Control Blocks were to be conflated into one and used for all columns of this memory. However, it is quite clear that at least what could be termed multiplexing arrangement of Clemons cannot be adapted to a memory of Kuroda in that sense, even when the fact that they are completely different memories are overlooked.

It seems wholly illogical by the standards of one of ordinary skill to transfer structural and operational details of the semiconductor SRAM of Clemons to the active matrix-addressable ferroelectric memory of Kuroda and certainly such an undertaking would not yield the present invention, which specifically is concerned with both limiting the number of sense amplifiers and obtaining a suitable high data rate by an appropriate segmenting of a word line and providing for reading each word line segment in parallel by using a sense amplifier block with the number of sense amplifiers equal to the number of bit lines defining a word line segment in order that a high data rate may be maintained and the number of sense amplifiers kept to manageable proportions, whereas the number of bit lines of the memory according to the present invention can be as large as desired.

Thus, Kuroda in combination with Clemons fails to teach, *inter alia,* each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment, as recited in claims 1, 12 and 13.

Appellant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness. Thus, Appellant maintains that claims 1, 12 and 13 are allowable over the combination of *Kuroda* and *Clemons* for at least the reason noted above.

VIII. CLAIMS

A copy of the claims involved in the present Appeal are attached hereto as Appendix A.

IX. EVIDENCE

There is no additional evidence pursuant to §§ 1.130, 1.131, or 1.132 and/or evidence entered by or relied upon by the examiner that is relevant to this appeal as noted in Appendix B.

X. RELATED PROCEEDINGS

There is no related proceedings known to Appellants.

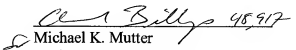
XI. CONCLUSION

The withdrawal of the outstanding rejections and the allowance of claims 1-5 and 12-18 are earnestly solicited.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, and 1.21 that may be required by this paper and to credit any overpayment to Deposit Account No. 02-2448.

Dated: June 24, 2008

Respectfully submitted,



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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/088,913 are as follows:

Claim 1. (Previously Presented)

A non-volatile passive matrix memory device comprising;

an electrically polarizable dielectric memory material exhibiting hysteresis, wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes, wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,

wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line, where each memory cell is at all times in physical contact with a word line and a bit line,

wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage larger than the coercive voltage Vc, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling

simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

Claim 2. (Previously Presented)

A non-volatile passive matrix memory device according to claim 1, wherein simultaneous connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Claim 3. (Previously Presented)

A non-volatile passive matrix memory device according to claim 2, wherein the number of multiplexers corresponds to the largest number of bit lines defining a segment, each bit line of a segment being connected with a specific multiplexer.

Claim 4. (Previously Presented)

A non-volatile passive matrix memory device according to claim 3, wherein the output of each multiplexer is connected with a single sensing means.

Claim 5. (Previously Presented)

A non-volatile passive matrix memory device according to claim 4, wherein the single sensing means is a sense amplifier.

Claims 6. – 11. (Withdrawn)

Claim 12. (Previously Presented)

A volumetric data storage apparatus comprising:

a plurality of stacked layers, each layer including one non-volatile passive matrix memory device, the non-volatile passive matrix memory device including an electrically polarizable dielectric memory material exhibiting hysteresis, wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes,

wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,

wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines,

wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line and where each memory cell is at all times in physical contact with a word line and a bit line, wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell,

wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage Vs, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with an a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same

position being sensed at the same time be said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

Claim 13. (Previously Presented)

A memory device, comprising:

a first set of electrodes which constitute word lines of the memory device;

a second set of electrodes which constitute bit lines of the memory device, the second set of electrodes being positioned substantially orthogonal to the first set of electrodes, the bit lines being divided into a number of segments;

an electrically polarizable dielectric memory material provided in a layer between the first and second set of electrodes, the electrically polarizable dielectric memory material and the first and second set of electrodes forming a passive matrix memory in which each memory cell can be selectively addressed for a write/read operation and where the memory material is at all times in physical contact with the first and second set of electrodes; and

a number of sensing devices connected to each of a corresponding bit lines within each segment of word lines, where each word line in each segment is differentiated based on the position of the word line within the segment, each word line of each segment being adjoined to a separate bit line, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing device from the number of sensing devices, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment.

Claim 14. (Previously presented)

A non-volatile passive matrix memory device according to claim 1, wherein the number of sensing means is equal to the number of bit lines within each segment, where each segment

contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing means.

Claim 15. (Previously presented)

A volumetric data storage apparatus according to claim 12, wherein the number of sensing means is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing means.

Claim 16. (Previously presented)

A memory device according to claim 13, wherein the number of sensing devices is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing device.

Claim 17. (Previously presented)

A non-volatile passive matrix memory device according to claim 1, wherein the electrically polarizable dielectric memory material is ferroelectric material.

Claim 18. (Previously presented)

A volumetric data storage apparatus according to claim 12, wherein the electrically polarizable dielectric memory material is ferroelectric material.

B

APPENDIX B

There is no additional evidence pursuant to §§ 1.130, 1.131, or 1.132 and/or evidence entered by or relied upon by the examiner that is relevant to this appeal.

C

APPENDIX C

There are no related proceedings.

D

APPENDIX D

Additional support material

Table 1;

A1;

B1;

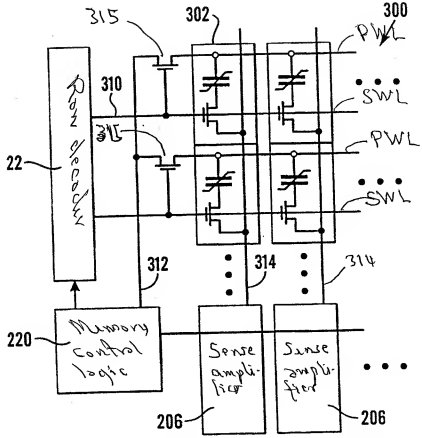
C1-C5; and

D1-D11.

Table 1

Table comparing the present invention with the cited prior art, Clemons and Kuroda, as well as the hypothetical modification of Kuroda as conjectured by the Examiner

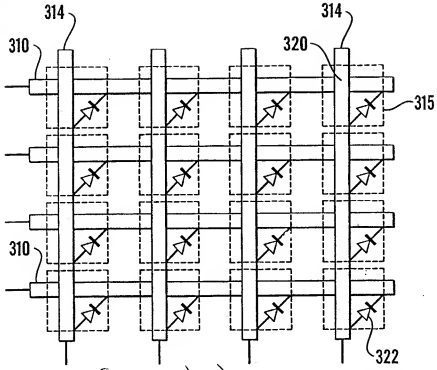
PATENT	CLEMONS	KURODA	HYPOTETHICAL MODIFICATION OF KURODA	PRESENT APPLICATION
Priority	February 17, 1984	August 27, 1993		August 24, 2000
Memory type	SRAM (Static Random Access Memory)	FEM (Ferroelectric Memory)	FEM (Ferroelectric memory)	FEM (Ferroelectric memory)
Architecture	Active matrix-addressable, columns of byte blocks	Active matrix-addressable, 1T-8C memory circuits, blocks of memory circuits provided in rows and columns	Active matrix-addressable, rows and columns of byte blocks	Passive matrix-addressable
Data organization	Bytewise	Bitwise	Bytewise	Word line segment
Parallel readout	1 byte, typical 8 bits	Not applicable	1 byte, typical 8 bits	Segment-wise, typical 1 K bit
Multiplex	Selects all bit lines of a column	Selects one data line in one column	Selects all data lines of a column	Selects all bit lines defining a word line segment
Number of multiplexers	1	One for each column, typical 8	1	1
Size of memory	Unknown	Typical 1024 memory cells (16 x 64)	Typical 1024 memory cells (16 x 64)	Typical 8K x 8K memory cells = 64 MK bits
Parallel read	Yes, 1 byte	No	Yes, 1 byte	Yes, word line segment (typical 1 Kbit)
Disturb	No	Limited to a memory circuit	Limited to all memory circuits of a block	All unselected memory cells
Disturb reduction	None	Voltage pulse protocol with 1/2 selection rule	Unknown	Voltage pulse protocol with 1/3 selection rule
Object of invention	Bytewise organization, parallel readout	Higher integration reduced disturb	Bytewise organization, parallel readout	Reduce number of sense amplifiers, maintain high specific data access rate ($\sim 10^9$ s-1) massive parallel access for readout
Advantage	Comprises spare bit lines, parallel readout	Increased integration compared with fully active FEM, reduced disturb compared with wholly passive FEM	Parallel readout, bytewise organization, number of sense amplifier corresponding of bit lines and word lines segment	High data rate, easy adaption to response time requirement, no limit to number of bit lines
Disadvantage	Slow, complex memory cell	No parallelism, slow, small, one multiplexer for each block column, disturb	8-fold increased disturb compared with Kuroda, may need improved voltage pulse protocol	All non-selected memory cells disturbed



Active ferroelectric memory (1T-1C cell)

Fig.3a

302 Memory
310 Select WL
312 Drive line, pulsing word line (PWL)
314 Bit line (Data line out)



Passive ferroelectric memory

Fig.3b

310 Word line } Plate lines
314 Bit line
315 Memory cell
320 Plate line crossing
322 Diode junction

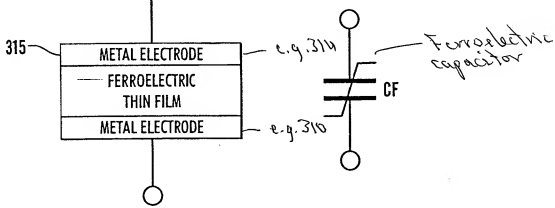


Fig.4

C/1

Static random access memory

From Wikipedia, the free encyclopedia

Static random access memory (SRAM) is a type of semiconductor memory where the word *static* indicates that it, unlike *dynamic* RAM (DRAM), does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data remanence,[1] but is still *volatile* in the conventional sense that data is eventually lost when the memory is not powered. The term SDRAM, which stands for *synchronous DRAM*, should not be confused with SRAM.

Computer memory types

Volatile

- DRAM, e.g. DDR SDRAM
- **SRAM**
- Upcoming
  - Z-RAM
  - TTRAM
- Historical
  - Williams tube
  - Delay line memory

Non-Volatile

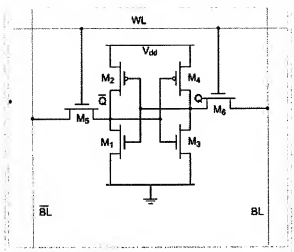
- ROM
  - PROM
  - EAROM
  - EPROM
  - EEPROM
- Flash memory
- Upcoming
  - FeRAM
  - MRAM
  - PRAM
  - SONOS
  - RRAM
  - NRAM
- Historical
  - Drum memory
  - Magnetic core memory
  - Bubble memory

Contents

Design

Random access means that locations in the memory can be written to or read from in any order, regardless of the memory location that was last accessed.

Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional *access* transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit[1] [2] [3] -- sometimes to implement more ports in a register file.



A six-transistor CMOS SRAM cell.

Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing a silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory.

Memory cells that use fewer than 6 transistors are possible -- but such 3T[4][5] or 1T cells are DRAM, not SRAM (even 1T-SRAM).

Access to the cell is enabled by the word line (WL in figure) which controls the two *access* transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: $\overline{BL}$ and BL. They are used to transfer data for both read and write operations. While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM speed compared to DRAMs—in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bitline to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signalling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down.

The size of an SRAM with m address lines and n data lines is 2^m words, or $2^m \times n$ bits.

SRAM operation

An SRAM cell has three different states it can be in: *standby* where the circuit is idle, *reading* when the data has been requested and *writing* when updating the contents. The three different states work as follows:

Standby

If the word line is not asserted, the *access* transistors M_5 and M_6 disconnect the cell from the bit lines. The two cross coupled inverters formed by $M_1 - M_4$ will continue to reinforce each other as long as they are disconnected from the outside world.

Reading

Assume that the content of the memory is a **1**, stored at Q. The read cycle is started by precharging both the bit lines to a logical **1**, then asserting the word line WL, enabling both the *access* transistors. The second step occurs when the values stored in Q and $\overline{Q}$ are transferred to the bit lines by leaving BL at its

precharged value and discharging $\overline{BL}$ through M_1 and M_5 to a logical **0**. On the BL side, the transistors M_4 and M_6 pull the bit line toward V_{DD}, a logical 1. If the content of the memory was a **0**, the opposite would happen and $\overline{BL}$ would be pulled toward **1** and BL toward **0**.

Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a **0**, we would apply a **0** to the bit lines, i.e. setting $\overline{BL}$ to **1** and BL to **0**. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. A **1** is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

Bus behaviour

A RAM memory with an access time of 70 ns will output valid data within 70 ns from the time that the address lines are valid. But the data will remain for a hold time as well (5-10ns). Rise and fall time also affect (~5ns). By reading the lower part of an address range bits in sequence (page cycle) one can read with significantly shorter access time (30ns). [2] It is also referred to as Shadow Random Access Memory.

Applications and Uses

Characteristics

SRAM is a little more expensive, but faster and significantly less power hungry (especially idle) than DRAM. It is therefore used where either speed or low power, or both, are principle considerations. SRAM is also easier to control (interface to) and generally more truly *random access* than modern types of DRAM. Due to a more complex internal structure, SRAM is less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.

Clock speed and power

The power consumption of SRAM varies widely depending on how frequently it is accessed; it **can** be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full speed. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draw very little power and can have a nearly negligible power consumption when sitting idle — in the region of a few microwatts.

Static RAM exists primarily as:

- general purpose products
  - with *asynchronous* interface, such as the 28 pin 32Kx8 chips (usually named XXC256), and similar products up to 16 Mbit per chip
  - with *synchronous* interface, usually used for caches and other applications requiring burst transfers, up to 18 Mbit (256Kx72) per chip
- integrated on chip

- as RAM or cache memory in microcontrollers (usually from around 32 bytes up to 128 kilobytes)
- as the primary caches in powerful microprocessors, such as the x86 family, and many others (from 8 KB, up to several megabytes)
- to store the registers and parts of the state-machines used in some microprocessors -- see register file
- on application specific ICs, or ASICs (usually in the order of kilobytes)
- in FPGAs and CPLDs (usually in the order of a few kilobytes or less)

Embedded use

Many categories of industrial and scientific subsystems, automotive electronics, and similar, contains static RAM. Some amounts (kilobytes or less) is also embedded in practically all modern appliances, toys, etc that implements an electronic user interface. Several mebibytes may be used in complex products such as digital cameras, cell phones, synthesizers, etc.

SRAM in its dual-ported form is sometimes used for realtime digital signal processing circuits.

In computers

SRAM is also used in personal computers, workstations, routers and peripheral equipment: internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc. LCD screens and printers also normally employ static RAM to hold the image displayed (or to be printed). Small SRAM buffers are also found in CDROM and CDRW drives; usually 256 KB or more are used to buffer track data, which is transferred in blocks instead of as single values. The same applies to cable modems and similar equipment connected to computers. The so called "CMOS RAM" on PC motherboards was originally a battery-powered SRAM chip, but is today more often implemented using EEPROM or Flash.

Hobbyists

Hobbyists often prefer SRAM due to the ease of interfacing. It is much easier to work with than DRAM as there are no refresh cycles and the address and data buses are directly accessible rather than multiplexed. In addition to buses and power connections, SRAM usually require only three controls: Chip Enable (CE), Write Enable (WE) and Output Enable (OE).

Types of SRAM

By transistor type

- Bipolar junction transistor (used in TTL and ECL) — very fast but consumes a lot of power
- MOSFET (used in CMOS) — low power and very common today

By function

- Asynchronous — independent of clock frequency; data in and data out are controlled by address transition
- Synchronous — all timings are initiated by the clock edge(s). Address, data in and other control

signals are associated with the clock signals

By feature

- ZBT (ZBT stands for zero bus turnaround) — the turnaround is the number of clock cycles it takes to change access to the SRAM from **write** to **read** and vice versa. The turnaround for ZBT SRAMs or the latency between read and write cycle is **zero**.
- syncBurst (syncBurst SRAM or synchronous-burst SRAM) — features synchronous burst write access to the SRAM to speed up write operation to the SRAM.

See also

- DRAM
- DIMM
- Flash memory

References

1. ^ Sergei Skorobogatov (June 2002). "*Low temperature data remanence in static RAM*". University of Cambridge, Computer Laboratory. Retrieved on 2008-02-27.
2. ^ Tentative Toshiba mos digital integrated circuit silicon gate cmos 4,194,304-word by 16-bit cmos pseudo static RAM. 070731 toshiba.com

- Digital Integrated Circuits - a design perspective. J. M. Rabaey, A. Chandrakasan, B. Nikolić. Prentice Hall, 2003. ISBN 0-13-120764-4.

External links

- Uses of SRAM by Intel Corp.

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Categories: Computer memory

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(54) **SEMICONDUCTOR MEMORY AND METHOD FOR ACCESSING SEMICONDUCTOR MEMORY**

(57) A method of accessing a semiconductor memory comprising ferroelectric memory FETs arranged as a matrix to allow to write and/or read data to and from only an intended memory cell without the data in not-intended cells being destroyed by the application of a disturbing voltage to not-intended cells, even without providing each cell with a selection element. The method is characterized in that, when data are written to or read from memory cells Q1 through Q4 arranged as a matrix comprising ferroelectric memory FETs each having a ferroelectric layer on the gate side to constitute a semiconductor memory, a voltage of a direction opposite that of the voltage for writing or reading the data is applied, followed by the application of a voltage for writing or reading.

FIG.1(a)

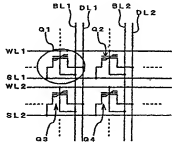


FIG.1(b)

	WL1	WL2	SL1	SL2	BL1	BL2	DL1	DL2
WRITE "1"	0	2/3Vcc			Vcc	1/3Vcc		
	Vcc	1/3Vcc			0	2/3Vcc		
WRITE "0"	Vcc	1/3Vcc			0	2/3Vcc		
	0	2/3Vcc			Vcc	1/3Vcc		
READ	-V1	0			0		-SA	
	V1	0			0		+SA	

EP 1 031 989 A1

Description

Cross Reference to Related Applications

[0001] The entire disclosure including the specifications, claims, drawings, and abstracts of Japanese patent applications Nos. Hei 9-313359, filed on November 14, 1997 and Hei 9-313360, filed on November 14, 1997 is incorporated herein by reference.

Technical Field

[0002] This invention relates to non-volatile semiconductor memory using ferroelectric capacitors, and more specifically to a semiconductor memory comprising ferroelectric memory FETs each having at least a ferroelectric layer between a gate electrode and a semiconductor layer, and to a method of gaining access to the semiconductor memory.

Background Art

[0003] A ferroelectric memory has for example an FET structure as shown in FIG. 14 in which a ferroelectric layer 54 and a gate electrode 55 are provided on part of a semiconductor substrate 51 between a drain region 52 and a source region 53 formed on a semiconductor substrate 51. It is known that; when a high voltage is applied between the gate electrode 55 and the semiconductor substrate 51, polarization charge is produced, and "1" or "0" is written depending on the direction of polarization; the data "1" or "0" can be read by applying a low voltage to the gate electrode; and the data do not disappear even if power is turned off. Therefore it is known that the device can be used as a non-volatile memory of non-destructive reading type. However, practical use of a memory is yet to be realized in which the above-described memory cells are arranged as a matrix circuit. That is, a method is known in which each of cells arranged as a matrix may be accessed through selection elements provided, two for each cell, one for writing and the other for reading. However, when two selection elements are used for each cell respectively, a problem arises that the cell area increases and the degree of integration extremely decreases.

[0004] On the other hand, an access method is considered for example for a memory made of matrix-arranged ferroelectric capacitors, in which a power source voltage Vcc is equally divided into three and applied to each line, in order to prevent a voltage from being applied to a cell other than an intended, selected cell at the time of writing for example and prevent the data from being rewritten. To apply the three equally divided voltage application method to a memory in which ferroelectric memory FETs are arranged as a matrix, the following access method may be considered.

[0005] That is, as shown in the simplified drawing FIG. 13(a), in the case cells comprising a plurality of ferroelectric memory FETs in matrix-pattern are wired and "1" is to be written to a selected cell P, the writing is carried out by applying Vcc to a word line WL1 on which the selected cell P is present, 1/3 of Vcc to a word line WL2 on which the selected cell P is absent, 0 to a bit line BL1 on which the selected cell P is present, and 2/3 · Vcc to a bit line BL2 on which the selected cell P is absent. In the case "0" is to be written to the selected cell P, 0 is applied to the word line WL1, 2/3 of Vcc to the word line WL2, Vcc to the bit line BL1, and 1/3 of Vcc to the bit line BL2. When the selected cell P is to be read, V1 (a voltage lower than Vcc at the time of reading) is applied to the word line WL1, 0 to the word line WL2, 0 to the bit line BL1, and V_{SA} (data detecting voltage) to a data line DL1. The sequence in writing and reading "1" and "0" is shown in FIG. 13(b). The blank boxes in FIG. 13(b) denote that the corresponding lines are open or at 0 V. As a result, when the writing is carried out, a high voltage of Vcc or —Vcc is applied between the gate electrode and the semiconductor substrate to write "1" or "0." At this time, the voltage applied to a cell not selected is 1/3 of Vcc or —1/3 of Vcc and writing is not carried out. At the time of reading, while V1 is applied between the gate electrode and the semiconductor substrate in selected cells, cells not selected are open or at 0 V, almost no voltage is applied, and no reading is carried out.

[0006] While writing and reading can be made by selecting only an intended cell as described above, at the time of writing for example, the voltage of 1/3 of Vcc is also applied to cells not selected. When the voltage 1/3 of Vcc is applied, polarization of ferroelectric capacitor (polarization corresponding to the stored data "1" or "0") is disturbed. After repeated applications, there is a concern that the data stored in cells to which no writing is made may change. Under such a circumstance, there are following problems: For the small-sized semiconductor memories using the ferroelectric memory cells, an access method without disturbing the data stored in the memory cells not selected is yet to be established. And as described above, a semiconductor memory has not yet been put to practical use in which the ferroelectric memory FETs are arranged as a matrix of cells.

Disclosure of the Invention

[0007] An object of this invention made to solve the above-described problems is to provide a method of writing and reading with a semiconductor memory constituted with ferroelectric memory FETs arranged as a matrix, allowing to write and/or read data to and from only a selected memory cell without the data being destroyed by a disturbing voltage applied to cells not selected without providing each cell with a selection element.

[0008] Another object of the invention is to provide a semiconductor memory having ferroelectric memory FETs constituted to be reliably used by restoring the

data even when the data are disturbed and deteriorated as a result of applying a low voltage to cells not selected as described above.

[0009] Still another object of the invention is to provide an access method with a semiconductor memory constituted with ferroelectric memory FETs arranged as a matrix, allowing to prevent stored data from being disturbed even with an access method in which a power source voltage is equally divided into three and applied.

[0010] That is to say, the object of the invention is providing a semiconductor memory, etc. using ferroelectric memory with which stored data are not disturbed.

[0011] According to the invention, a method of writing data to a semiconductor memory including a memory cell which comprises ferroelectric memory FETs each having a ferroelectric layer disposed between a gate electrode and a semiconductor layer is characterized in that a writing voltage is applied after applying a voltage that is opposite in direction to the writing voltage.

[0012] According to the invention, a method of reading data from a semiconductor memory including a memory cell which comprises ferroelectric memory FETs each having a ferroelectric layer disposed on gate electrode side is characterized in that a reading voltage is applied after applying a voltage that is opposite in direction to the reading voltage.

[0013] The term ferroelectric memory FET having a ferroelectric layer between a gate electrode and a semiconductor layer refers to any memory element of an FET structure with at least a ferroelectric layer disposed between a gate electrode and a semiconductor layer, such as a structure (MFS structure) of a gate electrode (metal M) - ferroelectric (F) - semiconductor (S); a structure in which at least one layer other than ferroelectric layer is disposed between the metal M and a semiconductor S of the MFS structure; and a structure (MFMIS structure) of a gate electrode (M) -ferroelectric (F) -floating gate (M)-insulation film (I) - semiconductor (S).

[0014] When the above-described method is used, even if the disturbing voltage of 1/3 of Vcc is applied to cells not selected in the access method of equally dividing the power source voltage into three and applying to respective lines, the decrease in charge due to the disturbing voltage is restored by the constant application of a voltage in the opposite direction to that of the disturbing voltage in succession, and the data are prevented from being removed.

[0015] The voltage application to each memory cell at the time of writing can be made such that for example the power source voltage is equally divided into three and applied to each line. In that case, it is possible to apply the power source voltage to a selected cell while applying ±1/3 of the power source voltage to cells not selected.

[0016] The above-mentioned memory can be constituted such that the memory cells made of the ferroelectric memory FETs are arranged as a matrix, gates of cells in a row in one direction are connected to form a word line, sources of cells in a row in one direction are connected to form a source line, drains of cells in a row in the other direction are connected to form a data line, and semiconductor layers of cells in a row in the other direction are connected to form a bit line. Writing and reading can be made by applying a voltage between the word line and the bit line.

[0017] The semiconductor memory using the ferroelectric layer of the invention comprises memory cells made of ferroelectric memory FETs each having a ferroelectric layer between a gate electrode and a semiconductor layer, buffer cells capable of transferring data from the memory cells, and buffer circuits that transfer data from a memory cell to a buffer cell and write the transferred data again to the memory cell.

[0018] This constitution allows to periodically refreshing data in the memory cell by the use of the buffer cell, so that the data are retained and prevented from disappearing over a long period of time.

[0019] This arrangement in which the memory cells are disposed as a matrix, the buffer cell comprises a row of cells capable of transferring data of at least one line of memory cells of lateral or vertical row of the memory cell, and the buffer circuit is capable of collectively transferring data of at least one line of the memory cell and also capable of writing again, allows it possible to transfer and write again data of every line at a time, so that data are refreshed within a short period of time.

[0020] If the buffer cell is made of a ferroelectric memory FET having a ferroelectric layer between a gate electrode and a semiconductor layer, dummy memory cells can be manufactured with the same process as that for the memory cells.

[0021] When the buffer circuit is constituted with a first selection element connected between the gate electrode of the buffer cell and the data line of the memory cell to control the transfer of the memory cell, a second selection element to read data from the buffer cell connected to the gate electrode of the buffer cell, and a transformer which transforms the voltage of the data read from the buffer cell and is connected to the bit line interconnecting the substrates of the memory cells, data can be refreshed any time by the control of the selection elements.

[0022] An access method for a semiconductor memory comprising memory cells made of ferroelectric memory FETs each having a ferroelectric layer between a gate electrode and a semiconductor layer, and buffer cells capable of transferring data of the memory cells is characterized in that the data of the memory cells are once transferred to the buffer cells and the transferred data are written again to the memory cells, so that the data of the memory cell are refreshed.

[0023] The refreshment of the data stored in the memory cells is preferably carried out either at constant time intervals depending on the disturbance characteristic obtained in advance for the data of the ferroelectric

layer used in the memory cell or every time the number of writings and/or readings data to and from the memory cell reaches a predetermined value. In this case, the number of accesses, or the number of readings and writings may be counted with a counter, so that the data are refreshed when the number reaches a predetermined value.

[0024] While the features of this invention can be broadly shown as described above, its constitution and contents together with its objects and other features will become further apparent from the following disclosure in reference to the appended drawings.

Brief Description of the Drawings

[0025]

FIG. 1(a) is a wire connection diagram of a semiconductor memory as an embodiment of the invention.
FIG. 1(b) is a table, showing an operation sequence of the semiconductor memory shown in FIG. 1(a).
FIG. 2 is an explanatory plan view, showing an example of a structure of a memory cell portion in FIG. 1.
FIGs. 3(a) to 3(d) are explanatory drawings of cross sections in FIG. 2.
FIG. 4 is an explanatory plan view, showing another example of a structure of the memory cell portion of FIG. 1.
FIGs. 5(a) to 5(d) are explanatory drawings of cross sections in FIG. 4.
FIGs. 6(a) to 6(d) show examples of the waveform applied to examine the disturbance characteristics.
FIG. 7 shows disturbance characteristics versus the number of pulses applied.
FIG. 8 shows changes in the charge at every application of positive and negative bidirectional pulses.
FIG. 9 shows change in the current versus time when voltages are applied to a ferroelectric capacitor.
FIG. 10 shows disturbance characteristics versus width of pulses applied.
FIG. 11 shows disturbance characteristics versus magnitude (amplitude) of pulses applied.
FIG. 12 shows an equivalent circuit diagram of a semiconductor memory as another embodiment of the invention.
FIGs. 13(a) and 13(b) are explanatory drawings of accessing matrix-arranged ferroelectric memory FETs using the three equally divided voltage method.
FIG. 14 is an explanatory drawing of a ferroelectric memory FET as an example.

Best Mode for Carrying out the Invention

[0026] Now the method of writing and reading to and from a semi conductor memory using a ferroelectric layer as an embodiment of this invention will be described in reference to the appended drawings.

[0027] The method of writing and reading to and from a semiconductor memory using a ferroelectric layer as an embodiment of this invention uses the semiconductor memory shown in FIG. 1(a) according to the sequence shown in FIG. 1(b). FIG. 1(a) shows part of the semiconductor memory including four memory cells Q1 to Q4 arranged as a matrix and made of ferroelectric memory FETs each having a ferroelectric layer between a gate electrode and a semiconductor layer. When selecting a memory cell and writing or reading data to or from the selected memory cell, the method as an embodiment of this invention is characterized in that a voltage of opposite direction to that of a voltage for writing or reading is applied before applying the voltage for writing or reading. That is, the applicant has found the following facts after repeating diligent studies and examinations: The influence of the disturbing voltage of 1/3 • Vcc applied to cells not selected on the data in the cell not selected was examined, for example when data are written by the method of equally dividing the power source voltage into three, through changes in the amount of charge in the ferroelectric capacitor. As a result, it has proved that, as will be described later, although the amount of charge in the ferroelectric capacitor is disturbed even when a low voltage is applied, the disturbing phenomenon is offset and the charge is restored by the application of an opposite directional disturbing pulse. Based on such findings, the characteristic of this invention lies in preventing the data from being deteriorated by the disturbing voltage when the data are written or read; the prevention is effected by applying an opposite directional voltage before applying the voltage for writing or reading.

[0028] Next, concrete examples will be described further in detail in reference to FIG. 1. FIG. 1(a) shows part of a matrix structure comprising four memory cells Q1 to Q4 made of ferroelectric memory FETs. Gate electrodes of cells arranged side by side in the lateral direction are connected and respectively provided with word lines WL1 and WL2. Sources of cells arranged side by side in the lateral direction are connected and respectively provided with source lines SL1 and SL2. Drains of cells arranged one over another in the vertical direction are connected and respectively provided with data lines DL1 and DL2. Substrates (semiconductor layers) of cells arranged one over another in the vertical direction are connected and respectively provided with bit lines BL1 and BL2. Thus, part of the matrix is formed.

[0029] To write "1" to a selected cell Q1, first, 0 is applied to the word line WL1 of the selected cell Q1, Vcc is applied to the bit line BL1 of the selected cell Q1, 2/3 of Vcc to the word line WL2 of a not-selected cell, and 1/3 of Vcc to the bit line BL2 (an opposite voltage to that for writing "1" is applied). Next, Vcc is applied to the word line WL1, 0 is applied to the bit line BL1, 1/3 • Vcc

FIG.13(a)

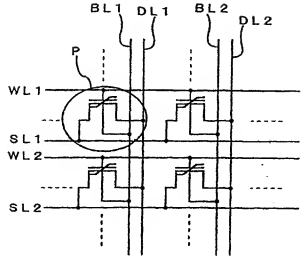
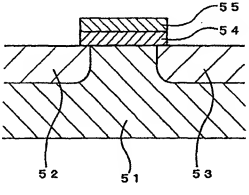


FIG.13(b)

	WL1	WL2	SL1	SL2	BL1	BL2	DL1	DL2
WRITE "1"	Vcc	1/3Vcc			0	2/3Vcc		
WRITE "0"	0	2/3Vcc			Vcc	1/3Vcc		
READ	V1	0			0		V_{SA}	

FIG.14



D/6

Ferroelectric RAM

From Wikipedia, the free encyclopedia

This article is about an information storage medium. For other uses, see Fram (disambiguation).

Ferroelectric RAM (**FeRAM** or **FRAM**[1]) is a type of non-volatile computer memory. It is similar in construction to DRAM, which is currently used in the majority of a computer's main memory, but uses a ferroelectric layer to achieve non-volatility. Although the market for non-volatile memory is currently dominated by Flash RAM, FeRAM offers a number of advantages, notably lower power usage, faster write speed and a much greater maximum number (exceeding 10^{16} for 3.3 V devices) of write-erase cycles.

Computer memory types

Volatile

- DRAM, e.g. DDR SDRAM
- SRAM
- Upcoming
  - Z-RAM
  - TTRAM
- Historical
  - Williams tube
  - Delay line memory

Non-Volatile

- ROM
  - PROM
  - EAROM
  - EPROM
  - EEPROM
- Flash memory
- Upcoming
  - **FeRAM**
  - MRAM
  - PRAM
  - SONOS
  - RRAM
  - NRAM
- Historical
  - Drum memory
  - Magnetic core memory
  - Bubble memory

FeRAM is currently one of several "advanced" non-volatile memory (NVRAM) technologies that are attempting to gain acceptance as an alternative to flash by avoiding its key weaknesses – high program and erase voltages, slow programming speed, write-erase endurance that is limited to ~10^5 cycles. Compared to its primary competitors among the new NVRAM technologies, MRAM and PRAM, FeRAM is more mature with volume production at Fujitsu beginning in 1999. FeRAMs at 1-Mbit densities were available in high volume in 2006 from both Fujitsu and Ramtron. Limited volume production of a 4-Mbit MRAM began at Freescale Semiconductor in July 2006, while PRAM has not yet entered volume production at any manufacturer. However, none of the new NVRAM come close to offering the high storage densities (now multiple gigabits) nor the low cost per storage bit of flash memory although PRAM is significantly higher then MRAM and FeRAM. FeRAM is competitive in specialized niche applications where its properties (low write voltage, fast write speed, and much greater write-erase endurance) give it a compelling advantage over flash memory.

Much of the current FeRAM technology was developed by Ramtron International. One major licensee is Fujitsu, who operate what is probably the largest semiconductor production line with FeRAM capability. Since 1999 they have been using this line to produce standalone FeRAMs, as well as specialized chips (e.g. chips for smart cards) with embedded FeRAMs within. Fujitsu also produces devices for Ramtron. Several other companies are known to be active in developing FeRAM. For example, since at least 2001 Texas Instruments (TI) has collaborated with Ramtron to develop FeRAM test chips in a modified 130 nm process. In the fall of 2005 Ramtron reported that they were evaluating prototype samples of an 8-Mbit FeRAM manufactured using TI's FeRAM process. Fujitsu and Seiko-Epson were in 2005 collaborating in the development of a 180 nm FeRAM process. FeRAM research projects have also been reported at Samsung, Matsushita, Oki, Toshiba, Infineon, Hynix, Symetrix, Cambridge University, University of Toronto and the Interuniversity Microelectronics Centre (IMEC, Belgium).

Contents

Description

Conventional DRAM consists of a grid of small capacitors and their associated wiring and signaling transistors. Each storage element, a *cell*, consists of one capacitor and one transistor, a so-called "1T-1C" device. DRAM cells scale directly with the size of the semiconductor fabrication process being used to make it. For instance, on the 90 nm process used by most memory providers to make DDR2 DRAM, the cell size is 0.22 μm^2, which includes the capacitor, transistor, wiring, and some amount of "blank space" between the various parts – it appears 35% utilization is typical, leaving 65% of the space wasted.

Data in a DRAM is stored as the presence or lack of an electrical charge in the capacitor, with the lack of charge generally representing "0". Writing is accomplished by activating the associated control transistor, draining the cell to write a "0", or sending current into it from a supply line if the new value should be "1". Reading is similar in nature; the transistor is again activated, draining the charge to a *sense amplifier*. If a pulse of charge is noticed in the amplifier the cell held a charge and thus reads "1", the lack of such a pulse indicates a "0". Note that this process is *destructive*, once the cell has been read, if it did hold a "1" it must be re-charged to that value again. Since a cell loses its charge after some time due to leak currents, it needs to be actively refreshed at intervals.

The 1T-1C storage cell design in an FeRAM is similar in construction to the storage cell in widely used DRAM in that both cell types include one capacitor and one access transistor. In a DRAM cell capacitor a linear dielectric is used whereas in an FeRAM cell capacitor the dielectric structure includes ferroelectric material, typically lead zirconate titanate (PZT).

As shown in the figure, a ferroelectric material has a nonlinear relationship between the applied electric field and the apparent stored charge. Specifically, the ferroelectric characteristic has the form of a hysteresis loop, which is very similar in shape to the hysteresis loop of ferromagnetic materials. The dielectric constant of a ferroelectric is typically much higher than that of a linear dielectric because of the effects of semi-permanent electric dipoles formed in the crystal structure of the ferroelectric material. When an external electric field is applied across a dielectric, the dipoles tend to align themselves with the field direction, produced by small shifts in the positions of atoms and shifts in the distributions of electronic charge in the crystal structure. After the charge is removed, the dipoles retain their polarization state. Typically binary "0"s and "1"s are stored as one of two possible electric polarizations in each data storage cell. For example, in the figure a "1" is encoded using the negative remnant polarization "-Pr", and a "0" is encoded using the positive remnant polarization "+Pr".

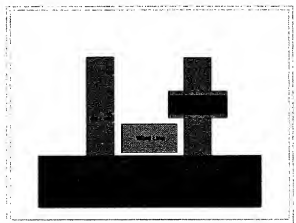
Operationally FeRAM is similar to DRAM. Writing is accomplished by applying a field across the ferroelectric layer by charging the plates on either side of it, forcing the atoms inside into the "up" or "down" orientation (depending on the polarity of the charge), thereby storing a "1" or "0". Reading, however, is somewhat different than in DRAM. The transistor forces the cell into a particular state, say "0". If the cell already held a "0", nothing will happen in the output lines. If the cell held a "1", the re-orientation of the atoms in the film will cause a brief pulse of current in the output as they push electrons out of the metal on the "down" side. The presence of this pulse means the cell held a "1". Since this process overwrites the cell, reading FeRAM is a destructive process, and requires the cell to be re-written if it was changed.

Generally the operation of FeRAM is similar to ferrite core memory, one of the primary forms of computer memory in the 1960s. In comparison, FeRAM requires far less power to flip the state of the polarity, and does so much faster. The requirement for a write cycle for each read cycle, together with the high but not infinite write cycle limit, poses a potential problem for some special applications.

Comparison with other systems

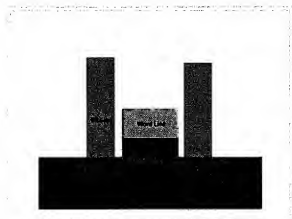
Density

The main determinant of a memory system's cost is the density of the components used to make it up. Smaller components, and less of them, means that more cells can be packed onto a single chip, which in turn means more can be produced at once from a single silicon wafer. This improves yield, which is directly related to cost.



Structure of a FeRAM cell.

The lower limit to this scaling process is an important point of comparison, generally the technology that scales to the smallest cell size will end up being the least expensive per bit. FeRAM and DRAM are constructionally similar, and can generally be built on similar lines at similar sizes. In both cases the lower limit seems to be defined by the amount of charge needed to trigger the sense amplifiers. For DRAM this appears to be a problem at around 55 nm, at which point the charge stored in the capacitor is too small to be detected. It is not clear if FeRAM can scale to the same size, as the charge density of the PZT layer may not be the same as the metal plates in a normal capacitor.



Structure of a 1 transistor FeRAM cell and its working mechanism.

That said, to date the only commercial FeRAM devices appear to have been produced on many-generations-old fabs, at 350 nm. Experimental processes at 180 nm and 130 nm are ongoing. Early models required two FeRAM cells per bit, leading to very low densities, but this limitation has since

been removed.

Power consumption

The key advantage to FeRAM over DRAM is what happens *between* the read and write cycles. In DRAM, the charge deposited on the metal plates leaks across the insulating layer and the control transistor, and disappears. In order for a DRAM to store data for anything other than a microscopic time, every cell must be periodically read and then re-written, a process known as *refresh*. Each cell must be refreshed many times every second (~65 ms[2]) and this requires a continuous supply of power.

In contrast, FeRAM only requires power when actually reading or writing a cell. The vast majority of power used in DRAM is used for refresh, so it seems reasonable to suggest that the benchmark quoted by TTR-MRAM researchers is useful here too, indicating power usage about 99% lower than DRAM.

Another non-volatile memory type is Flash RAM, and like FeRAM it does not require a refresh process. Flash works by pushing electrons across a high-quality insulating barrier where they get "stuck" on one terminal of a transistor. This process requires high voltages, which are built up in a charge pump over time. This means that FeRAM could be expected to be lower power than Flash, at least for writing, as the write power in FeRAM is only marginally higher than reading. For a "mostly-read" device like the iPod nano the difference might be slight, but for devices with more balanced read and write, like a digital camera, the difference could be expected to be much higher.

Speed

DRAM speed is limited by the speed at which the current stored in the cells can be drained (for reading) or stored (for writing). Generally this ends up being defined by the capability of the control transistors, the capacitance of the lines carrying power to the cells, and the heat that power generates.

FeRAM is based on the physical movement of atoms in response to an external field, which happens to be extremely fast, settling in about 1 ns. In theory, this means that FeRAM could be much faster than DRAM. However, since power has to flow into the cell for reading and writing, the electrical and switching delays would likely be similar to DRAM overall. It does seem reasonable to suggest that FeRAM would require less charge than DRAM, because DRAMs need to *hold* the charge, whereas FeRAM would have been written to before the charge would have drained. That said, there is a delay in writing because the charge has to flow through the control transistor, which limits current somewhat.

In comparison to Flash the advantages are much more obvious. Whereas the read operation is likely to be similar in performance, the charge pump used for writing requires a considerable time to "build up" power, a process that FeRAM does not need. Flash memories commonly need about 1 ms to write a bit, whereas even current FeRAMs are at least 100 times that speed.

The theoretical performance of FeRAM is not entirely clear. Existing 350 nm devices have read times on the order of 50 to 60 ns. Although slow compared to modern DRAMs, which can be found with times on the order of 2 ns, common 350 nm DRAMs operated with a read time of about 35 ns,[3] so FeRAM performance appears to be comparable given the same fab.

Overall

FeRAM remains a relatively small part of the overall semiconductor market. In 2005 worldwide semiconductor sales were US $235 billion (according to the Gartner Group), with the flash memory market accounting for US $18.6 billion (according to IC Insights). The 2005 annual sales of Ramtron, perhaps the largest FeRAM vendor, were reported to be US $32.7 million. Flash memory is currently the overwhelmingly dominant NVRAM technology, and this situation seems likely to continue for at least the rest of the decade. The much larger sales of flash memory compared to the alternative NVRAMs support a much larger research and development effort. Flash memory is produced using the latest semiconductor linewidths (e.g. 70 nm at Samsung in 2006) whereas production FeRAMs are produced in linewidths that are several generations older (e.g. 350 nm at Fujitsu in 2006). Flash memory cells can store multiple bits per cell (currently 2 in the highest density NAND flash devices), and the number of bits per flash cell is projected to increase to 4 or even to 8 as a result of innovations in flash cell design. The areal bit densities of flash memory are consequently much higher than FeRAM, and thus the cost per bit of flash memory is orders of magnitude cheaper than FeRAM.

FeRAM, as well as the other emerging NVRAMs, must find niche markets where their advantages over flash memory (e.g. faster write speed and greater write-erase endurance) offset their higher cost and smaller storage densities. The density of FeRAM arrays should be increased by improvements in FeRAM processing technology and cell structures, such as the development of vertical capacitor structures (in the same way that DRAM cells use vertical cell structures to reduce the area of the cell footprint while maintaining a sufficiently strong data signal from the cell). Both the existing and new markets for FeRAM need to be exploited to support increased levels of research and development spending. In its 2005 annual meeting Ramtron reported significant sales of its FeRAM products in a variety of sectors including (but not limited to) electronic metering, automotive (e.g. black boxes, smart air bags), business machines (e.g. printers, RAID disk controllers), instrumentation, medical equipment, industrial microcontrollers, and radio frequency identification tags. Ramtron's product mix might not be representative of the overall FeRAM market; however, its sales numbers give a useful indication of the wide variety of possible applications of FeRAM. The other emerging NVRAMs, such as MRAM, may seek to enter similar niche markets in competition with FeRAM. According to Gartner, the flash memory market grew at an annual rate of 20% in 2005. Judging from Ramtron's released sales numbers, in 2005 the FeRAM market was probably growing at least as fast as the flash memory market and probably faster. The company is projecting annual sales growth in the range of from 30 to 35% in 2006 and 2007 across its diversified FeRAM product line.

It is possible to make FeRAM cells using two additional masking steps during conventional CMOS semiconductor manufacture, leading to the possibility of full integration of FeRAM into other chips. Flash typically requires nine masks. This makes FeRAM particularly attractive as an embedded non-volatile memory on microcontrollers, where the simpler process can reduce costs. However, the materials used to make FeRAMs are not commonly used elsewhere in integrated circuit manufacturing. Both the PZT ferroelectric layer and the noble metals used for electrodes raise process compatibility and contamination issues.

References

1. ^ FRAM is a registered trademark of Ramtron International Corporation. FRAM is used by Ramtron and its licencees to refer to FeRAM technology developed by Ramtron. FeRAM is the accepted generic acronym for ferroelectric random-access memory.
2. ^ http://download.micron.com/pdf/technotes/ddr2/TN4716.pdf

3. ^ http://ieeexplore.ieee.org/Xplore/login.jsp?url=/iel2/662/5918/00229238.pdf?tp=&arnumber=229238&isnumber=5918

See also

- Stabilizing ferroelectric materials
- Ferroelectric effect
- lead zirconate titanate
- MRAM
- nvSRAM
- EEPROM
- Phase-change memory
- Radio Frequency Identification
- Smart card
- Microcontroller
- Black box (disambiguation)#transportation

External links

- FRAM technology overiew by RAMTRON
- FeRAM Tutorial

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